UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/560,364	04/28/2000	Karen Lo	10002496-1	3565

22879 7590 03/12/2004

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
PERILLA, JASON M	
ART UNIT	**PAPER NUMBER**
2634	8

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/560,364	LO ET AL.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6 and 11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 6, and 11-15 are pending in the instant application.

Response to Arguments

2. Applicant's arguments, see page 14, filed December 12, 2003, with respect to the rejection(s)of claim(s) 1-2 under 35 U.S.C. § 102(b) have been fully considered and are persuasive *in view of the amendments to the claims*. Therefore, the rejection has been withdrawn.

Regarding the arguments with respect to the rejection(s)of claim(s) 1-2 under 35 U.S.C. § 102(b), the following response is made by the examiner. The argument that the reference, National Semiconductor DS26C31T/DS26C31M CMOS Quad TRI-STATE Differential Line Driver (National), does not receive, buffer, or otherwise process or generate data strobe signals is not convincing. In contrast, the examiner notes that the logic circuits of National are perfectly suited for the reception of and generation of data strobe signals. The term "data strobe signal" does not limit the claim to anything other than digital "data". Indeed, the logic of National is perfectly suited for transmitting differential digital logic levels regardless of what the logic levels represent including a "digital strobe signal". Further, the logic of National does more than simply buffer the signals because it creates a differential output. In short, National did meet the limitations of claim 1 as it was written during the first office action response. However, with the amendment of December 12, 2003, National does not meet the limitation, "wherein said data strobe transmit logic halt each said one or more data strobe signals

in a *selective* state". Therefore the previous rejection(s)of claim(s) 1-2 under 35 U.S.C. § 102(b) are withdrawn.

However, upon further consideration, a new ground(s) of rejection is made in view of National Semiconductor DS26C31T/DS26C31M CMOS Quad TRI-STATE Differential Line Driver in view of Texas Instruments CDC111 1-Line to 9-Line differential LVPECL Clock Driver and in further view of Texas Instruments CDC328A 1-Line to 6-Line Clock Driver with Selectable Polarity.

3. Applicant's arguments, see page 15, filed December 12, 2003, with respect to claims 11-15 have been fully considered but they are not persuasive.

Regarding the arguments with respect to the rejection(s) of claim(s) 6 and 11-15 under 35 U.S.C. § 102(a), the following response is made by the examiner. The argument that the reference Keeth et al (6026051) does not disclose or teach a data strobe transmit logic configured to generate a differential data strobe is not persuasive. In fact, Keeth et al discloses exactly a data strobe transmit logic configured to generate a differential data strobe. Figure 3 of Keeth et al clearly shows transmit logic (the outputs DCLK0OUT and DCLK0OUT* are configured to "transmit" internal to the RAM) to generate a differential (two opposite outputs DCLK0OUT and DCLK0OUT*) data strobe (abstract; line 4; "differential clock"). Further, Keeth et al discloses a strobe stopping signal and strobe stopping logic (fig. 3, ref. "enable*, 36, 44). The inverters 36 and 44 are strobe stopping logic. Also, it is inherent that there is "logic" that produces the enable* signal disclosed in figure 3, and it is strobe stopping logic. While the applicant notes that the logic of figure 3 is contained within a RAM circuit, the examiner

notes that the location of the logic is irrelevant. Indeed, the logic of figure 3 meets the limitations of the claims, and the rejection(s)of claim(s) 6 and 11-15 under 35 U.S.C. § 102(a) are again presented below.

4. Independent claim 4 is listed in the amended listing of the claims filed December 12, 2003. However, on page 15 of the remarks, the claim is described as canceled (paragraph 6). The examiner disregards the statement that claim 4 is canceled because it is listed contained in the claims listing and claim 6 depends on claim 4.

5. The previous rejection of claim 6 as anticipated by Keeth et al under 35 U.S.C. § 102(a) has been withdrawn because it failed to note the dependency upon claim 4. However, upon further consideration, a new ground(s) of rejection is made in view of Texas Instruments CDC111 1-Line to 9-Line differential LVPECL Clock Driver.

Claim Objections

6. Claim 3 recites the limitation "said first data strobe signal" in lines 1 and 3. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 3 recites the limitation "said second data strobe signal" in lines 2 and 4. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 11 recites the limitation "said signal generator logic" in line 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Texas Instruments CDC111 1-Line to 9-Line differential LVPECL Clock Driver (Texas-'111).

Regarding claim 4, Texas-'111 discloses a source synchronous transmitter constructed and arranged to transmit differential data strobe signals over a source synchronous communication link at a first frequency, with the differential data strobe signals toggling between two logical states at said first frequency when operating in a normal mode of operation and with the differential data strobe signals held at one of the logical states when operating in a data capture debug mode of operation. The CDC111 part is a source synchronous transmitter. The logic diagram on page 2 shows the source synchronous transmitter with differential outputs (YO and /Y0) and the function table on page 1 shows the normal mode of operation (/OE at low logic level) where the differential outputs toggle between one of two logical states and the debug mode of operation (/OE at high logic level) where the differential outputs are held at one of the two logical states.

Regarding claim 6, Texas-'111 discloses the limitations of claim 4 as applied above. Further, Texas-'111 also discloses the transmitter comprising data strobe transmit logic configured to generate said at least one data strobe as a differential data strobe (page 2 – logic diagram; outputs 25 and 24 are differential) comprising a data strobe signal (25) and an inverse data strobe signal (24). Texas-'111 also discloses

that the data strobe transmit logic comprises a differential data strobe signal generator configured to determine logical levels of said data strobe signal and said inverse data strobe signal, and strobe stopping logic (/OE) that controls a plurality of logic level signals (page 1 – function table) utilized by said signal generator to cause said data strobe signals to remain halted in a desired state. The logic diagram on page 2 clearly discloses the data strobe transmit logic comprising differential data strobe signal generators.

11. Claims 11-15 are rejected under 35 U.S.C. 102(a) as being anticipated by Keeth et al (6026051).

Regarding claim 11, Keeth et al discloses a differential data strobe transmitter (fig. 3) for transmitting over a source synchronous communication link a differential strobe comprising a data strobe signal and an inverse data strobe signal with a data signal, comprising, a differential data strobe (differential outputs DCLK0OUT and DCLK0OUT*) signal generator (fig. 3, ref. 38, 40, 46, & 48) that determines a shape of said data strobe signal and said inverse data strobe signal waveforms (inherent), and strobe stopping logic (fig. 3, ref. 36, 44) configured to control signal level states used by said signal generator logic (fig. 3, ref. 38, 40, 46, & 48) to cause said data strobe signal and said inverse data strobe signal to remain halted in a desired state (col. 3, lines 45-51; col. 4, lines 49-65). The enable signal itself is one of the control signal level states used to determine the output of the data strobe signal. Hence, it is utilized to directly control the signal level states used by the signal generator logic. It is inherent that the signals DCLK0OUT and DCLK0OUT* are transmitted over a communications link

internal to the RAM (abstract). Keeth et al also discloses the data signal that is transmitted with the data strobe signal. Figure 1 shows a "DATA LINK" between the memory controller (12) and the SLDRAM (10). The "DATA LINK" is also transmitted in the SLDRAM between the DATA LATCH (30) and the R/W CIRCUITRY (22).

Regarding claim 12, Keeth et al discloses the limitations as applied to claim 11 above, and further discloses the differential strobe signal generator logic selecting alternately between two applied signal levels to generate each of two differential data strobe signals. Figure 3 shows the differential strobe signal generator logic (ref. 38, 40, 46, & 48) having four applied signals (2 each per strobe output) used to generate the two differential data strobe signals. The 4 applied signals shown in figure 3 are:

1.) The output of inverter 36.

2.) The output of inverter 44.

3.) VCC connected to MUX 46.

4.) GND connected to MUX 40.

Keeth et al discloses that the two differential strobe outputs are each generated by selecting alternately between two of the applied signal levels (col. 3, line 45 – col. 4, line 65).

Regarding claim 13, Keeth et al discloses the limitations as applied to claim 12 above, and further discloses (col. 3, line 45 – col. 4, line 65) and shows in figure 3 that two applied signals levels (VCC & output of inverter 44) are used to generate strobe output DCLKOUT and two other applied signal levels (GND & output of inverter 36) are used to generate strobe output /DCLKOUT.

Regarding claim 14, Keeth et al discloses the limitations as applied to claim 12 above, and further discloses a first and third input signal to the differential data strobe generator held constantly in an asserted state (fig. 3, ref. VCC & the output of inverter 36) during normal operation as well as a second and forth input signal to the differential data strobe generator held constantly in a de-asserted state (fig. 3, ref. GND & the output of the inverter 44) during normal operation. Keeth et al also discloses that the differential signal generator selects alternately between the first and second input signals to generate the first data strobe signal and between the third and forth signals to generate the inverse data strobe signal (fig. 3; col. 3, line 45 – col. 4, line 65).

Regarding claim 15, Keeth et al discloses the limitations as applied to claim 12 above, and further discloses that the data strobe signal and the inverse data strobe signal are each generated as single ended bits that are opposite in phase with each other (col. 3, line 45 – col. 4, line 65).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-3, are rejected under 35 U.S.C. 103(a) as being anticipated by National Semiconductor DS26C31T/DS26C31M CMOS Quad TRI-STATE Differential Line Driver (National) in view of Texas-'111 and in further view of Texas Instruments CDC328A 1-Line to 6-Line Clock Driver with Selectable Polarity (Texas-'328A)

Regarding claim 1, National discloses a source synchronous link comprising a communication link and a source synchronous receiver and transmitter coupled to the communication link (page 6; "Two-Wire Balanced System, RS-422"). National further discloses the source synchronous transmitter comprising data transmit logic configured to manage the transmission of data signals over at least one data line of said communication link, and data strobe logic configured to generate one or more data strobes signals over a corresponding one or more clock line of said communication link, wherein said data strobe transmit logic halts each said one or more data strobe signals in a state in response to an external condition. The connection diagram on page one of the "Dual In-Line Package" shows four individual drivers. Any one of the four drivers is capable of the transmission of data signals over a data line, and any other of the four drivers is capable of the transmission of data strobe signals. According to the "Two-Wire Balanced System, RS-422" of page 6, a communication link is shown between transmission and reception logic. This communication link is the same communication link that would be used for both the transmission of data signals as a data line of the link as well as the clock line of the communications link for the transmission of data strobe signals. Therefore, National discloses "data transmit logic (any one of 6 line drivers) configured to manage the transmission of data signals over at least one data line (pg. 6) of said communication link, and data strobe logic (any one of 6 line drivers) configured to generate one or more data strobes signals over a corresponding one or more clock line of said communication link (pg. 6)". Further, National discloses on page 1 a logic or "Truth Table" which describes the various inputs and outputs of the data logic and the

data strobe logic. It is shown by the "Truth Table" on page 1 of National that by de-asserting the ENABLE inputs of the drivers, the data strobe transmit logic can be halted in response to an external condition. The truth table shows that as the ENABLE inputs are de-asserted (an external condition), the outputs of the data strobe transmit logic will be halted in a high impedance state "Z". National does not disclose that in response to an external condition, the outputs of the data strobe transmit logic can be held in a *logical* state. While National discloses that the outputs may be held in a state of High Impedance "Z", it does not disclose that it is capable of halting in a logical state. However, Texas-'111 does disclose a differential data strobe transmitter that transmits in one of two logical states in normal operation and at one of the logical states when operating in a data debug or halted mode. The function table on page 1 shows that the data strobe transmission logic transmits in one of the two logical states in normal operation (/OE at low logic level) and holds the data strobe transmission at one of the two logical levels when in the debug mode of operation (/OE at high logic level). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to modify the data strobe transmission logic of National to transmit one of two logical states used during normal operation when in a halted mode because the data strobe transmission should never be held in a state other than one of the two logical states used during normal transmission to ensure the proper interpretation of the data strobe signal at all times on the side of the receiver.

Further regarding claim 1, National in view of Texas-'111 discloses that the outputs may be held in a logical state when halted, but it does not disclose that it is

capable of halting in a *selected* logical state. However, Texas-'328A teaches a line driver with selectable polarity on the outputs. Page 2 of Texas-'328A shows a logic diagram with four line drivers. The "Function Table" of page 1 describes that the polarity control inputs (T/C) can be used to change the polarity of the output with respect to the input of the line drivers. Therefore, the state of the output of the line drivers can be *selected* with respect to the input. The drivers of National in view of Texas-'111 and Texas-'328A are analogous. One skilled in the art is capable of noting the benefits of selectable output levels with respect to input values. The description of the driver of Texas-'328A on page 1 recites, "Through the use of polarity-control inputs, various combinations of true and complementary outputs can be obtained." Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize selectable logic outputs (even in the non-enabled state) of Texas-'328A in the driver logic of National in view of Texas-'111 because various combinations of true and complementary outputs can be obtained. It is obvious that selectable logic outputs could be useful not only in the enabled state, but also in the non-enabled state so that various outputs could be obtained depending on system requirements.

Regarding claim 2, National in view of Texas-'111 and in further view of Texas-'328A discloses the limitations of claim 1 as applied above. Further, National discloses that the one or more data strobe signal(s) that comprise a first data strobe signal and a second data strobe signal that are transmitted with a phase opposite of each other (see

description of *differential* line driver). Figure 2 shows the waveforms of the data strobe (OUTPUT) and the phase opposite waveform (/OUTPUT) to be transmitted.

Regarding claim 3, National in view of Texas-'111 and in further view of Texas-'328A discloses the limitations of claim 1 as applied above. Further, Texas-'111 does disclose a differential data strobe transmitter that transmits in one of two logical states in normal operation and at one of the logical states when operating in a data debug or halted mode. The function table on page 1 shows that the data strobe transmission logic transmits in one of the two logical states in normal operation (/OE at low logic level) and holds the data strobe transmission at one of the two logical levels when it is halted (/OE at high logic level). The function table on page 1 also shows that one of the two data strobe signals is held at one of two logical states (Yn) and the second of two data strobe signals is held at the second of two logical states (/Yn).

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (703) 305-0374. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (703) 305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Jason M Perilla
February 19, 2004

jmp